Master Thesis

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Performance Driven Optimizations in FPGA Based QAM Systems
Introduction and Motivation

- Challenges in the current trend
  - Pursuit of high SNR and high data rate
  - Contribution to reach future terabit’s communication
  - FPGAs clocked below 1GHz: need for parallelism
Introduction and Motivation

- My work: performance optimization of QAM transmitter
  - Exploiting parallelism
  - FPGA platform
  - Mixed-domains (time and frequency) approach

- Current state-of-the-art
  - 2012: 128.6 MHz achieved (University of Shanghai, China) [2]
    - Transmitter and receiver
    - On Xilinx Virtex IV
  - 2013: 625.0 MHz achieved (University of Paderborn, Germany) [3]
    - Only transmitter
    - On Xilinx Virtex VI
  - 2015: 750.0 MHz achieved (E2v Semiconductor, UK) [4]
    - Only transmitter and no filter
    - On Xilinx Virtex VI
Introduction and Motivation

- **Hardware Choice**
  - **FPGA** because of great configurability, flexibility and cost
  - Growing technology

- **Modulation Choice**
  - **Quadrature Amplitude Modulation (QAM)**
  - Allow carrying many bits per symbol

- **Filter Choice**
  - Avoid Inter Symbol Interferences (ISI)
  - Finite impulse response (FIR)
  - Squared Raised Root Cosine (SRRC)
  - No filter optimizations in this work [5]
Outline

- **Introduction and Motivation**
- **Fundamentals**
  - Standard transmission chain
  - Fundamentals of each block
- **Concepts & Methodology**
  - Strategy
  - Ideal model
- **Implementation**
  - Implementation of each block
- **Experimental Results**
  - Achieved precision
  - Achieved performances
- **Summary & Further Improvements**
Fundamentals

- Standard Transmission Chain

Generator

Encryptor

Encoder

Smb. mapper

Filter

Modulator

Decryptor

Decoder

Smb. demapper

Filter

Demodulator

Channel

- Focus of this work
  - QAM mapper
  - Filter
  - Modulator
Fundamentals

- **QAM Mapper**
  - M-QAM formats (M=8, 16, 32, etc.)
  - Clusterization in \(\log_2(M)\) bits
  - Gray code for hamming distance of 1
  - Rectangular constellation is considered
  - Large \(M\) implies higher data rate
  - But symbol’s misinterpretation

- **Modulator**
  - Local oscillator delivering trigonometric orthogonal carriers
  - Multiplication and subtraction operation

\[
\text{out}(t) = \Re \{ [I(t) + iQ(t)]e^{2\pi f_0 t} \} \\
= I(t) \cos(2\pi f_0 t) - Q(t) \sin(2\pi f_0 t)
\]
Fundamentals

Fourier Transform

- Signal’s decomposition into an alternative representation
- Discrete Fourier Transform (DFT) sends it in the Fourier domain
- Inverse Discrete Fourier Transform (IDFT) takes it back

\[
X[k] = \sum_{n=0}^{N-1} x[n] e^{-2\pi i kn/N} \quad k \in \mathbb{Z}
\]

\[
x[n] = \frac{1}{N} \sum_{k=0}^{N-1} X[k] e^{2\pi i kn/N} \quad n \in \mathbb{Z}
\]

- Linear operations have equivalent in Fourier domain
- Useful for this work: convolution becomes multiplication

\[
\mathcal{F}\{f \ast g\} = \mathcal{F}\{f\} \cdot \mathcal{F}\{g\} \quad f \ast g = \mathcal{F}^{-1}\{\mathcal{F}\{f\} \cdot \mathcal{F}\{g\}\}
\]

\[
= G \cdot F \quad = \mathcal{F}^{-1}\{G \cdot F\}
\]
Fundamentals

Filter

- Nyquist criteria avoids ISI
- Pulse Shaping Filter to limit the transmission band
- FIR filter: linear phase, inherent stability, no feedback
- Matched filter improves SNR (if only stochastic noises)
- Good compromise: SRRC filter

Time Domain

\[ y[n] = x[n] \ast h[n] \]

- Convolution: difficultly parallelizable

Frequency Domain

\[ Y[k] = X[k] \cdot H[k] \]

- Multiplication: easily parallelizable

\[ H_0 \quad H_1 \quad \ldots \quad H_N \]

\[ X_0 \quad X_1 \quad \ldots \quad X_N \]

\[ Y_0 \quad Y_1 \quad \ldots \quad Y_N \]
Concepts & Methodology

- **Strategy**
  - Reference MATLAB model
  - Identify which part to implement in frequency domain
  - Prototype a single channel (non parallel) transmitter
  - Optimize for Xilinx Virtex 7
  - Generic model with parallelization and scalability

- **Conceptual Model**

![Diagram of QAM system with FIR filters and DFT/IDFT stages]
**Concepts & Methodology**

- **Ideal Behaviour**

![Diagram](image_url)

- **I component**
- **Q component**
- **DFT re. part**
- **DFT im. part**
- **FIR Filter**
- **IDFT re. part**
- **IDFT im. part**
- **Carriers’s frequency f_0**

**Equations:**

- $c_0 = 0.022507907$
- $c_1 = 0.028298439$
- $c_2 = -0.07620194$
- $c_3 = -0.03750077$
- $c_4 = 0.307673479$
- $c_5 = 0.540985931$

**Transmitter out**
Implementation

Implemented System

Data Packing

- Parallel inputs/outputs packed into the same bus
- Precision fixed to 16 bits
- Each $data_i$ is a 16-bit vector
Implementation

Specifications

<table>
<thead>
<tr>
<th>Latency</th>
<th>17 cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameters</td>
<td>N</td>
</tr>
<tr>
<td></td>
<td># of parallel inputs</td>
</tr>
<tr>
<td>FORMAT</td>
<td>QAM format</td>
</tr>
<tr>
<td>Inputs</td>
<td>clk</td>
</tr>
<tr>
<td></td>
<td>Clock</td>
</tr>
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<td></td>
<td>Validity flag</td>
</tr>
<tr>
<td>out</td>
<td>Output data</td>
</tr>
</tbody>
</table>

Characteristics

- Input width: (FORMAT x N)
- Output width: 16N
- Uses $2N^2$ complex multipliers, $4N^2-2N$ adder and $4N$ multipliers
Implementation

- **QAM Mapper**

  - Three parameters (N, W, FORMAT): number of inputs, bus width, QAM format
  - 8-QAM, 16-QAM, 32-QAM, 64-QAM support
  - Each format implemented in a separated Verilog file
  - Generates only the circuit for the desired format
Implementation

DFT & IDFT

- One parameter (N): number of inputs
- No parallel DFT / IDFT Xilinx IP cores available yet
- Each one uses $N^2$ complex multipliers and $2N(N-1)$ adders
- Rescaling of $2^{17}$ to fit the 16-bit bus
Implementation

- **Filter**

  - One parameter (N): number of inputs
  - Frequency domain: simple multiplication with filter coefficients
  - Uses 2N multipliers
  - Rescaling of $2^{16}$ to fit the 16-bit bus
### Implementation

**Modulator**

- One parameter (N) : number of inputs
- Uses 2N multipliers and N adders (configured in subtracter mode)
- Rescaling of $2^{16}$ to fit the 16-bit bus
Implementation

Fourier QAM Modulator (FQM) Utility

- Filter's coefficients
- Add & remove rows
- Carrier's frequency
- Summary
- Generate files
Experimental Results

- **Test Conditions**
  - N = 16, 100 Hz carriers
  - Different configurations for Adders and Multipliers cores
  - All supported QAM formats

- **Design Precision**
  - Less than 1% error respect to MATLAB!

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### Transmitter Output

![Transmitter Output Graph](image)

- **Data**
- **MATLAB**

### Transmitter Output Error

![Transmitter Output Error Graph](image)

- **Magnitude**
- **Samples**

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Alberto Sonnino – Performance driven optimization in FPGA based QAM systems
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Experimental Results

- **Final Result**
  - Adders using the fabric and Multipliers using DSP Slices

  | Slice Registers   | 5% |
  | Slice LUTs        | 7% |
  | LUTs Used as Logic| 6% |
  | Occupied Slices   | 17%|
  | Unused Flip Flop  | 28%|
  | Unused LUTs       | 51%|
  | Fully Used LUT-FF pairs | 19% |
  | Bounded IOBs      | 46%|
  | BUFG-BUFGCTRLs    | 6% |
  | DSP48E1s          | 57%|

- **Effective speed of** $16 \times 62.5 = 1 \text{ GHz}$ (instead of 750 MHz [3])

  - 8-QAM: $3 \times 16 \times 62.5 = 3 \text{Gb/s}$
  - 16-QAM: $4 \times 16 \times 62.5 = 4 \text{Gb/s}$
  - 32-QAM: $5 \times 16 \times 62.5 = 5 \text{Gb/s}$
  - 64-QAM: $6 \times 16 \times 62.5 = 6 \text{Gb/s}$

- **Throughput per modulation formats:**
Summary & Further Improvements

- **Topic**
  - Performance optimization of QAM transmitter
  - Exploiting parallelism using a mixed-domain approach

- **Achieved during this term**
  - Familiarization with Xilinx tools
  - Understanding of the underlying physical concepts
  - MATLAB simulation and prototyping a single-cannel transmitter
  - Build and optimize the parallel design
  - Scalable generic model

- **Further improvements**
  - Implement FFT instead of DFT (or wait for next Xilinx release)
  - Reduce the DSP utilization to allow $N = 32$
  - Support additional modulation formats
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Thank you for your attention!