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Master Thesis

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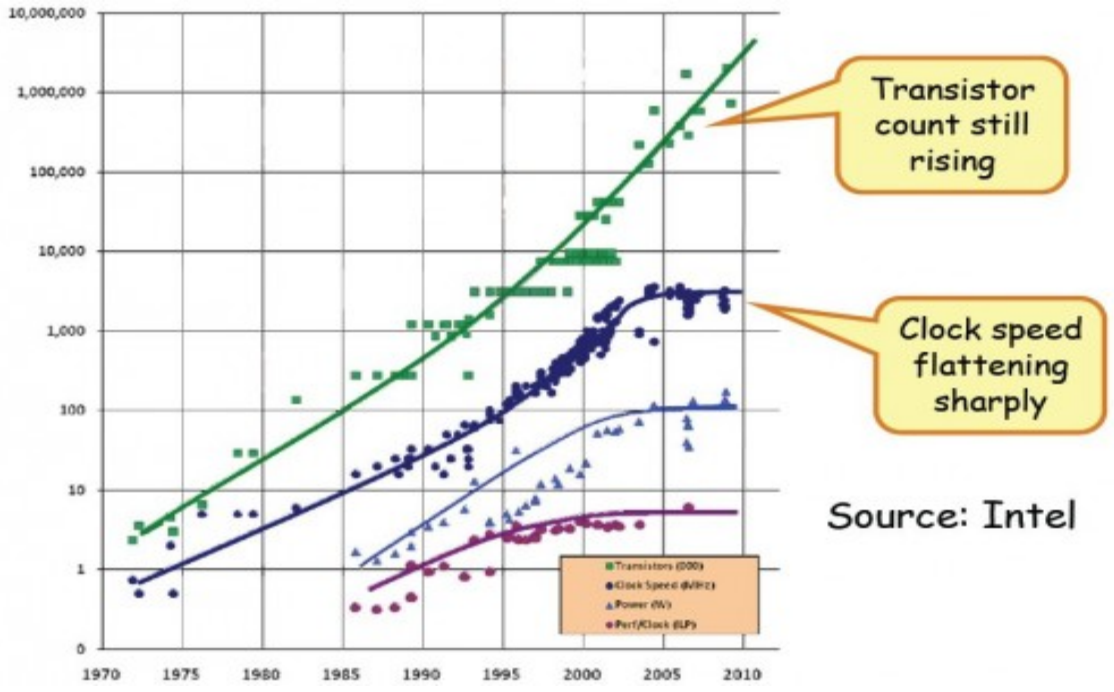
Performance Driven Optimizations in FPGA Based QAM Systems

Introduction and Motivation

- Challenges in the current trend
  - Pursuit of high SNR and high data rate
  - Contribution to reach future terabit's communication
  - FPGAs clocked below 1GHz: need for parallelism



Introduction and Motivation

- My work: performance optimization of QAM transmitter
  - Exploiting parallelism
  - FPGA platform
  - Mixed-domains (time and frequency) approach

- Current state-of-the-art
  - 2012: 128.6 MHz achieved (University of Shanghai, China) [2]
    - Transmitter and receiver
    - On Xilinx Virtex IV
  - 2013: 625.0 MHz achieved (University of Paderborn, Germany) [3]
    - Only transmitter
    - On Xilinx Virtex VI
  - 2015: 750.0 MHz achieved (E2v Semiconductor, UK) [4]
    - Only transmitter and no filter
    - On Xilinx Virtex VI

Introduction and Motivation

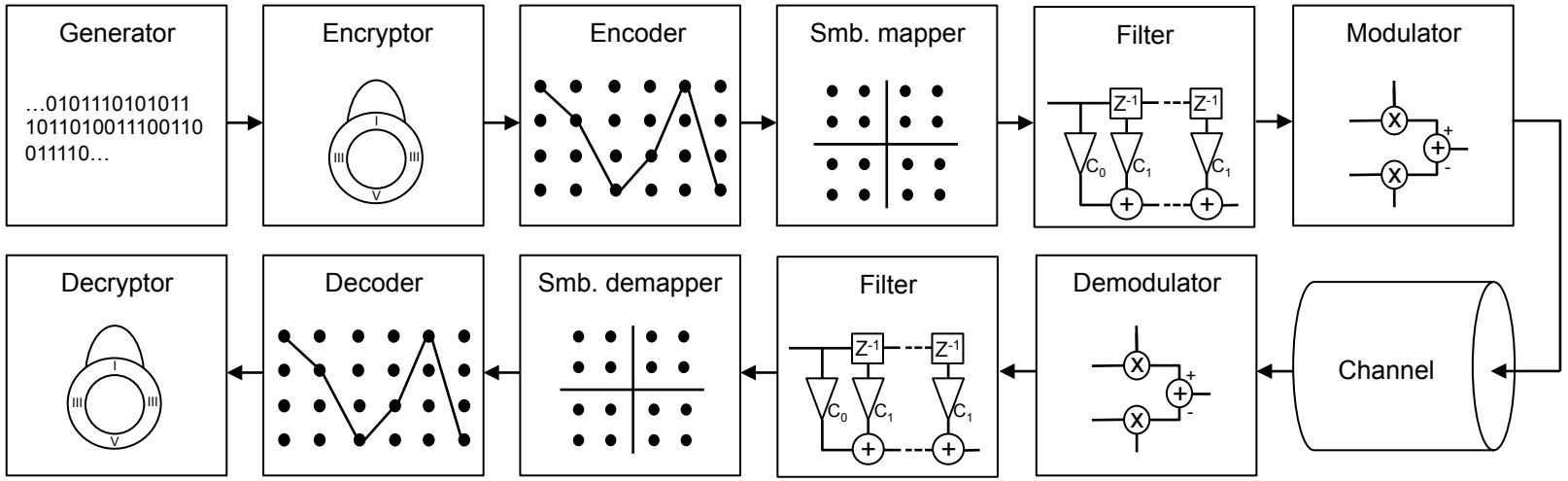
- Hardware Choice
  - FPGA because of great configurability, flexibility and cost
  - Growing technology
- Modulation Choice
  - Quadrature Amplitude Modulation (QAM)
  - Allow carrying many bits per symbol
- Filter Choice
  - Avoid Inter Symbol Interferences (ISI)
  - Finite impulse response (FIR)
  - Squared Raised Root Cosine (SRRC)
  - No filter optimizations in this work [5]

Outline

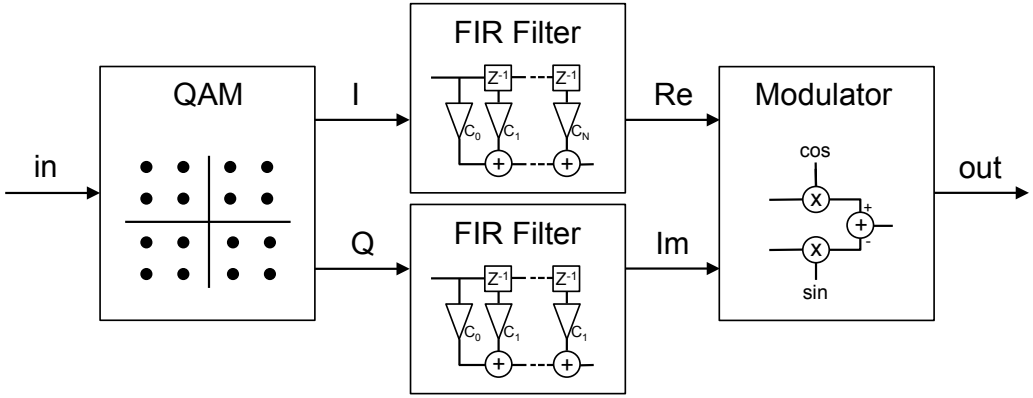
- Introduction and Motivation
- Fundamentals
  - Standard transmission chain
  - Fundamentals of each block
- Concepts & Methodology
  - Strategy
  - Ideal model
- Implementation
  - Implementation of each block
- Experimental Results
  - Achieved precision
  - Achieved performances
- Summary & Further Improvements

Fundamentals

- Standard Transmission Chain

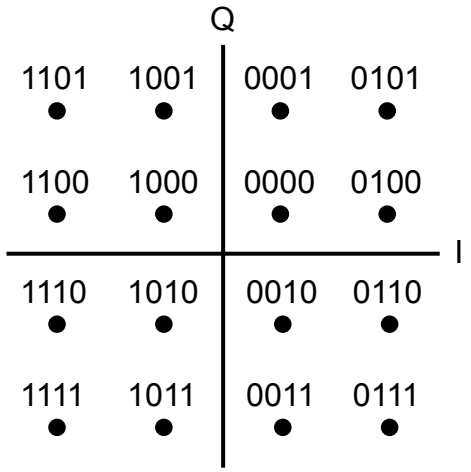


- Focus of this work
  - QAM mapper
  - Filter
  - Modulator



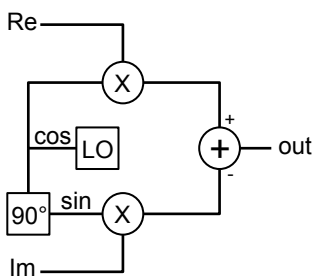
Fundamentals

- QAM Mapper
  - M-QAM formats (M=8, 16, 32, etc.)
  - Clusterization in $\log_2(M)$ bits
  - Gray code for hamming distance of 1
  - Rectangular constellation is considered
  - Large M implies higher data rate
  - But symbol's misinterpretation



- Modulator
  - Local oscillator delivering trigonometric orthogonal carriers
  - Multiplication and subtraction operation

$$\begin{aligned} out(t) &= \mathcal{R}\left\{[I(t)+iQ(t)]e^{2\pi f_0 t}\right\} \\ &= I(t)\cos(2\pi f_0 t) - Q(t)\sin(2\pi f_0 t) \end{aligned}$$



Fundamentals

- Fourier Transform
  - Signal's decomposition into an alternative representation
  - Discrete Fourier Transform (DFT) sends in the Fourier domain
  - Inverse Discrete Fourier Transform (IDFT) takes it back

$$X[k] = \sum_0^{N-1} x[n] e^{-2\pi i k n/N} \qquad k \in \mathcal{Z}$$

$$x[n] = \frac{1}{N} \sum_0^{N-1} X[k] e^{2\pi i k n/N} \qquad n \in \mathcal{Z}$$

  - Linear operations have equivalent in Fourier domain
  - Useful for this work: convolution becomes multiplication

$$\begin{aligned} \mathcal{F}\{f * g\} &= \mathcal{F}\{f\} \cdot \mathcal{F}\{g\} \\ &= G \cdot F \end{aligned} \qquad \begin{aligned} f * g &= \mathcal{F}^{-1}\{\mathcal{F}\{f\} \cdot \mathcal{F}\{g\}\} \\ &= \mathcal{F}^{-1}\{G \cdot F\} \end{aligned}$$

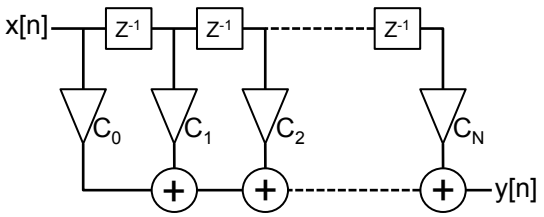
Fundamentals

- Filter
  - Nyquist criteria avoids ISI
  - Pulse Shaping Filter to limit the transmission band
  - FIR filter: linear phase, inherent stability, no feedback
  - Matched filter improves SNR (if only stochastic noises)
  - Good compromise: SRRC filter

Time Domain

$$y[n] = x[n] \circledast h[n]$$

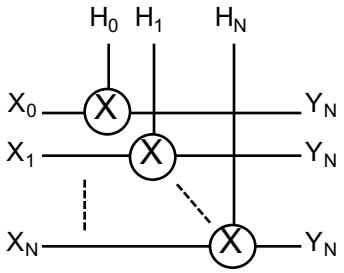
- Convolution: difficultly parallelizable



Frequency Domain

$$Y[k] = X[k] \cdot H[k]$$

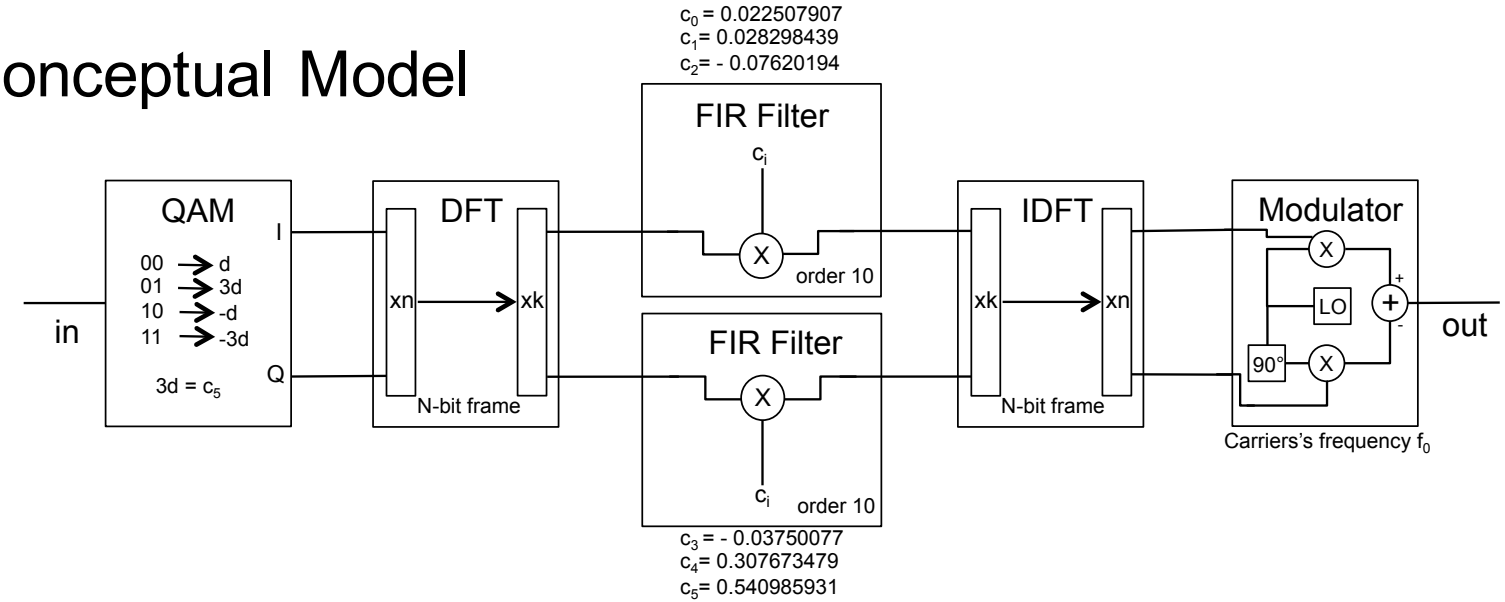
- Multiplication: easily parallelizable



Concepts & Methodology

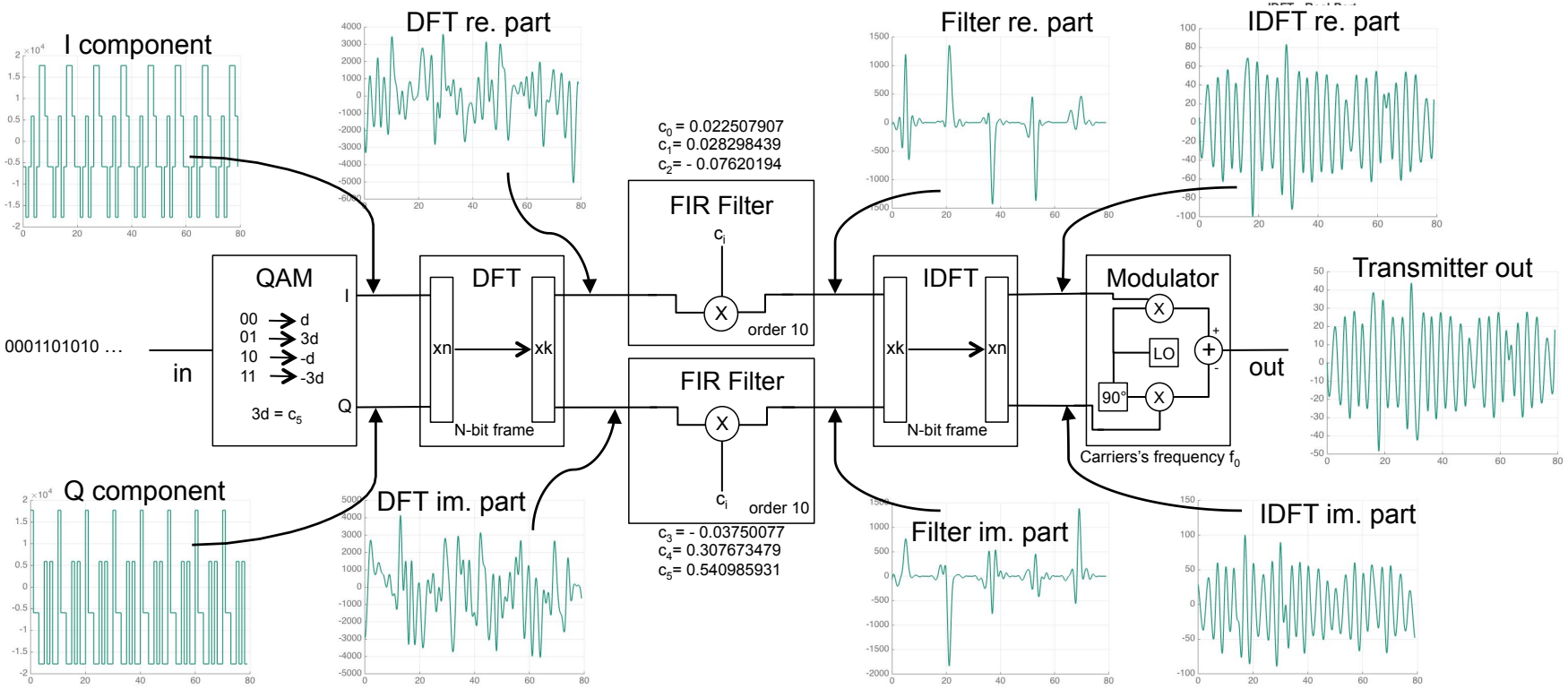
- Strategy
  - Reference MATLAB model
  - Identify which part to implement in frequency domain
  - Prototype a single channel (non parallel) transmitter
  - Optimize for Xilinx Virtex 7
  - Generic model with parallelization and scalability

- Conceptual Model



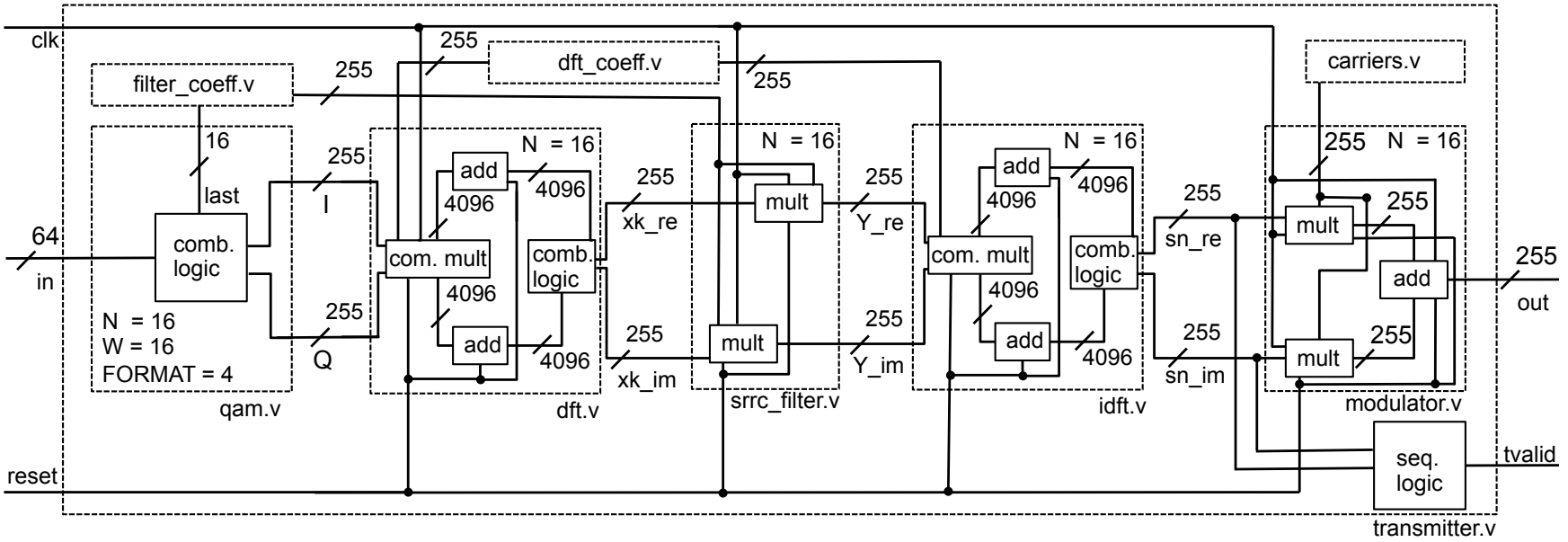
Concepts & Methodology

- Ideal Behaviour

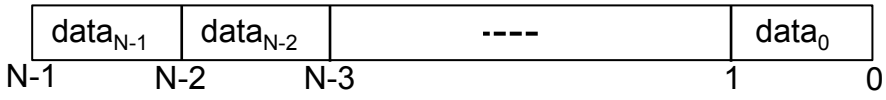


Implementation

- Implemented System



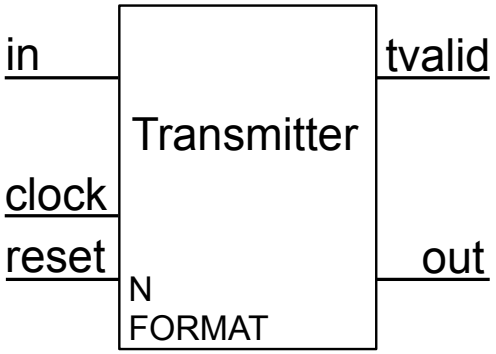
- Data Packing
  - Parallel inputs/outputs packed into the same bus
  - Precision fixed to 16 bits
  - Each $data_i$ is a 16-bit vector



Implementation

- Specifications

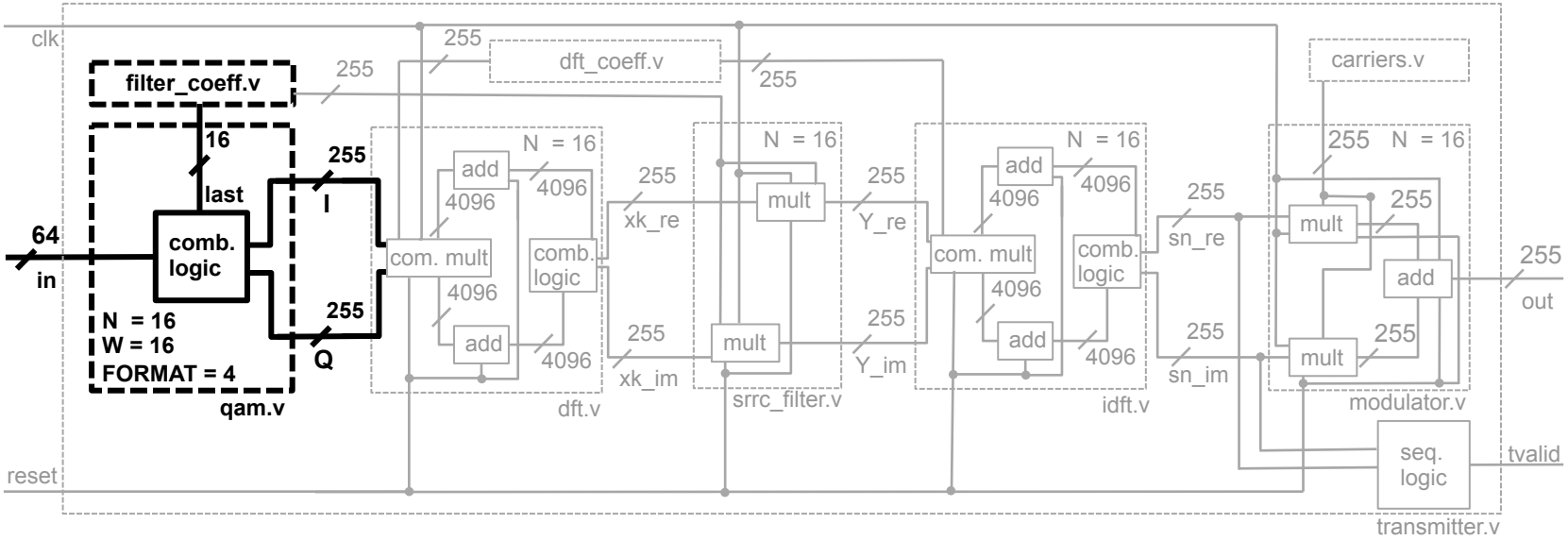
Latency	17 cycles	
Parameters	N	# of parallel inputs
	FORMAT	QAM format
Inputs	clk	Clock
	reset	Reset
	in	Cluseterd stream
Outputs	tvalid	Validity flag
	out	Output data



- Characteristics
  - Input width: (FORMAT x N)
  - Output width: 16N
  - Uses $2N^2$ complex multipliers, $4N^2$-2N adder and 4N multipliers

Implementation

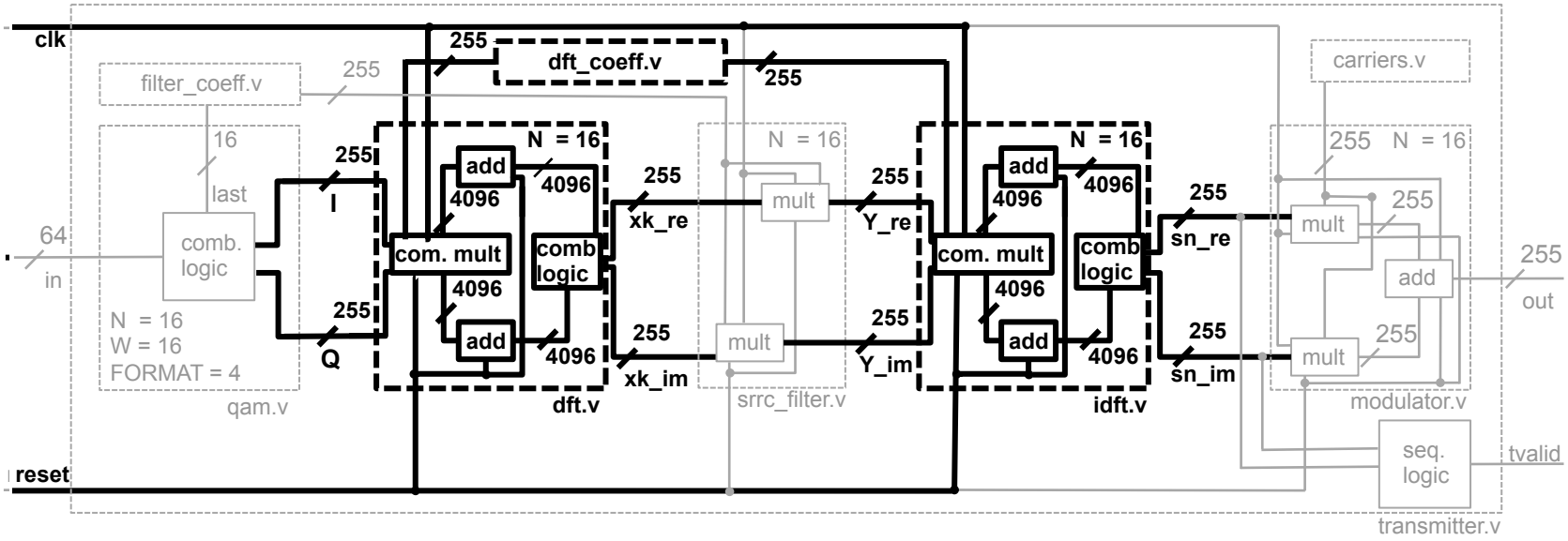
- QAM Mapper



- Three parameters (N, W, FORMAT): number of inputs, bus width, QAM format
- 8-QAM, 16-QAM, 32-QAM, 64-QAM support
- Each format implemented in a separated Verilog file
- Generates only the circuit for the desired format

Implementation

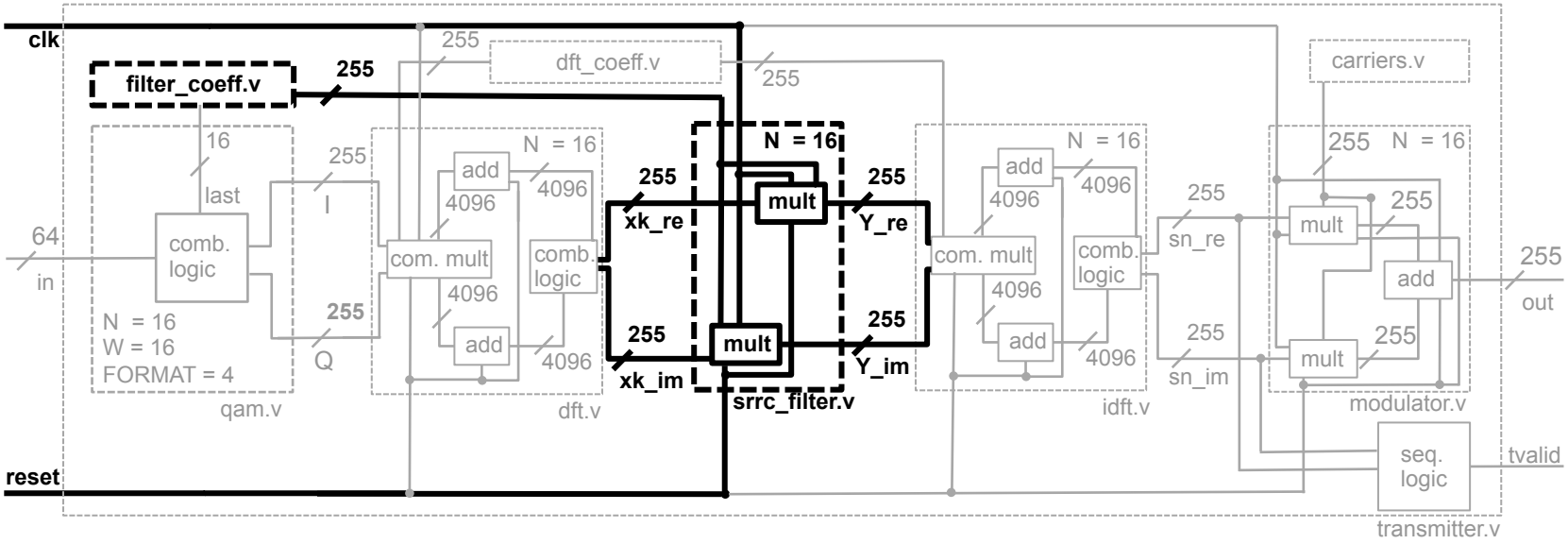
- DFT & IDFT



- One parameter (N) : number of inputs
- No parallel DFT / IDFT Xilinx IP cores available yet
- Each one uses N^2 complex multipliers and 2N(N-1) adders
- Rescaling of 2^{17} to fit the 16-bit bus

Implementation

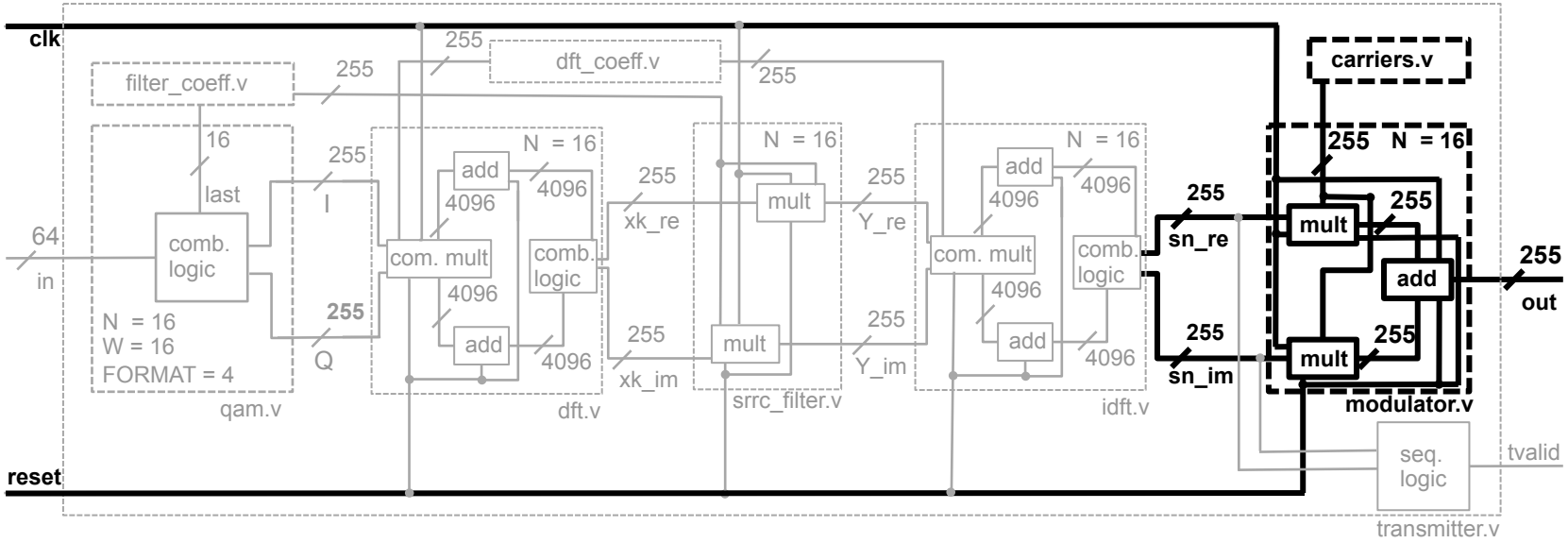
- Filter



- One parameter (N) : number of inputs
- Frequency domain: simple multiplication with filter coefficients
- Uses 2N multipliers
- Rescaling of 2^{16} to fit the 16-bit bus

Implementation

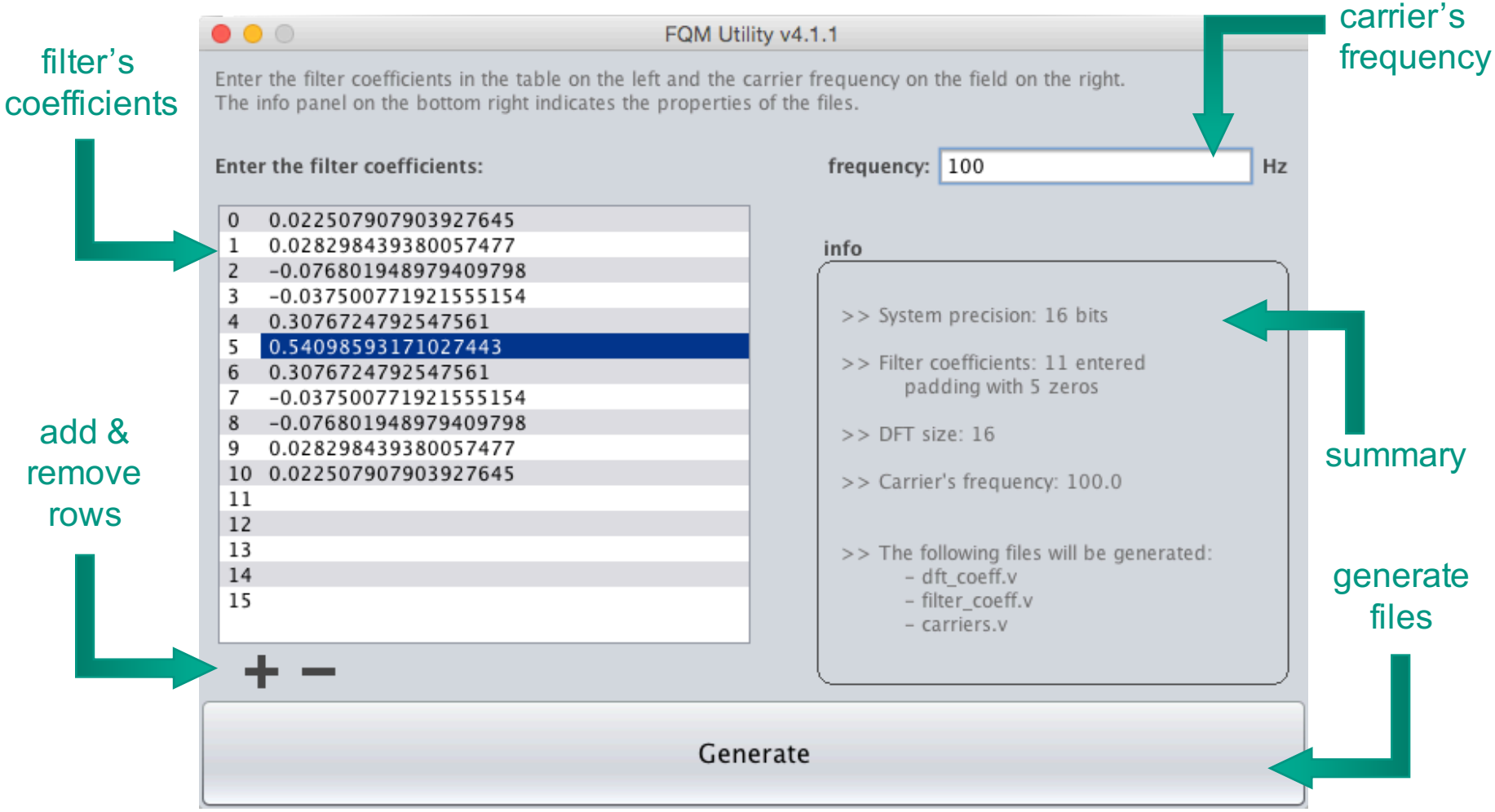
- Modulator



- One parameter (N) : number of inputs
- Uses 2N multipliers and N adders (configured in subtracter mode)
- Rescaling of 2^{16} to fit the 16-bit bus

Implementation

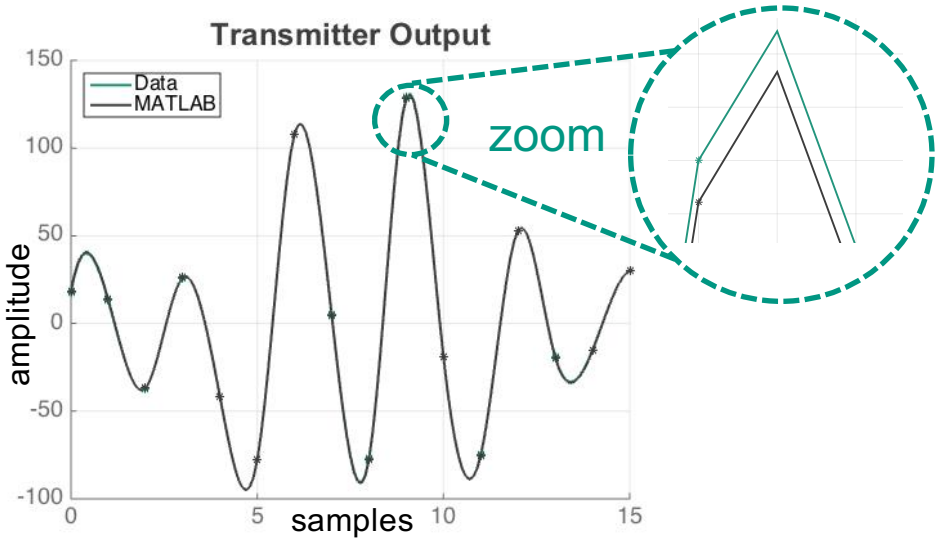
- Fourier QAM Modulator (FQM) Utility

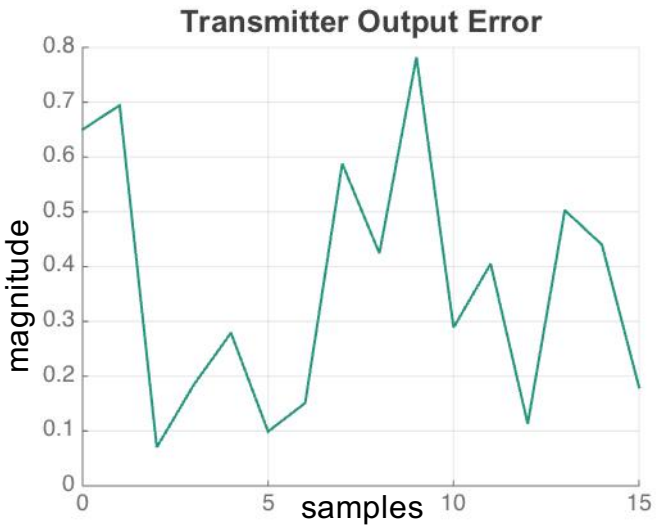


Experimental Results

- Test Conditions
  - N = 16, 100 Hz carriers
  - Different configurations for Adders and Multipliers cores
  - All supported QAM formats

- Design Precision
  - Less than 1% error respect to MATLAB !

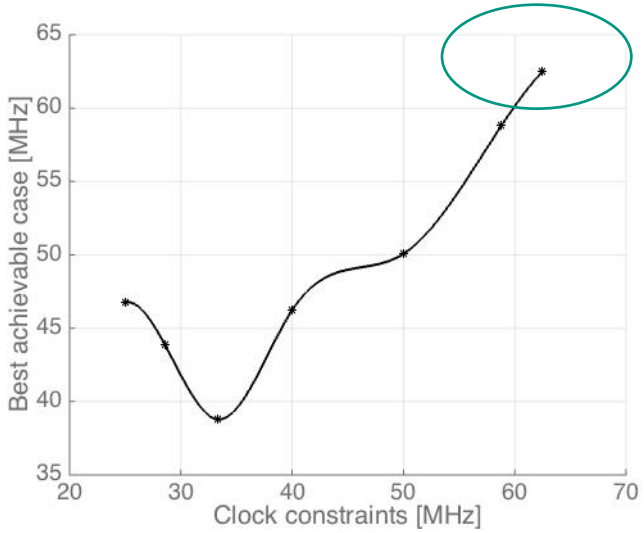




Experimental Results

- Final Result
  - Adders using the fabric and Multipliers using DSP Slices

Slice Registers	5%
Slice LUTs	7%
LUTs Used as Logic	6%
Occupied Slices	17%
Unused Flip Flop	28%
Unused LUTs	51%
Fully Used LUT-FF pairs	19%
Bounded IOBs	46%
BUFG-BUFGCTRLs	6%
DSP48E1s	57%



  - Effective speed of 16 x 62.5 = 1 GHz (instead of 750 MHz [3])
  - Throughput per modulation formats:

$$\begin{cases} 8-\text{QAM} : 3*16*62.5 = 3Gb/s \\ 16-\text{QAM} : 4*16*62.5 = 4Gb/s \\ 32-\text{QAM} : 5*16*62.5 = 5Gb/s \\ 64-\text{QAM} : 6*16*62.5 = 6Gb/s \end{cases}$$

Summary & Further Improvements

- Topic
  - Performance optimization of QAM transmitter
  - Exploiting parallelism using a mixed-domain approach
- Achieved during this term
  - Familiarization with Xilinx tools
  - Understanding of the underlying physical concepts
  - MATLAB simulation and prototyping a single-cannel transmitter
  - Build and optimize the parallel design
  - Scalable generic model
- Further improvements
  - Implement FFT instead of DFT (or wait for next Xilinx release)
  - Reduce the DSP utilization to allow N = 32
  - Support additional modulation formats

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Thank you for your attention !